Remarks

In the Office Action dated 11/28/2005 ("Office Action"), Claims 1-32 were rejected. In the Amendment set forth above, Claim 1, 12, 22, and 30 are amended, and the remaining Claims are as originally presented. In view of the amendments to the Claims and the remarks set forth below, it is respectfully submitted that all Claims are in condition for Allowance.

1. Claims 1, 3-4 and 6-10 were rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 5,911,149 to Luan et al. ("Luan"). This rejection is respectfully traversed.

Claim 1 describes a memory system having two storage devices (i.e., "first" and at least one "additional" storage devices) and that includes the following:

> a control storage device to store a programmable indicator identifying the manner in which the first and the at least one additional storage device are to be referenced; and
>
> a control circuit coupled to the first storage device, the at least one additional storage device, and the control storage device, the control circuit to receive a request for data, wherein copies of the requested data may be stored within the first and the at least one additional storage device, and in response to the request, to attempt to retrieve the requested data by initiating, based on the state of the programmable indicator, at least one of a first reference to the first storage device and a second reference to the at least one additional storage device.

The Examiner states that the Luan system controller 201 teaches Applicants' control storage device and a Luan memory configuration controller 202 teaches Applicants' control circuit. (Office Action page 2.) Applicants' Representative disagrees for the following reasons:

1. Applicants' control circuit is coupled to the first storage device and *at least one additional storage device*. The Examiner asserts that Applicants' additional memory is taught by the Luan dedicated peripheral memory 107 shown in the prior art system of Luan Figure 1A. (Office Action page 2.) However, this "additional storage device" of Luan is not coupled to the Luan

"control circuit" (said by the Examiner to be the memory configuration controller 202. In fact, this "additional storage device" is not even included in the same system as the control circuit. The "additional storage device" is contained in the prior art system of Luan Figure 1A, whereas the memory configuration controller 202 is included in the Luan of Figure 2. Thus, the Luan control circuit is coupled to exactly one memory 104, and not to any additional memory, as is clearly shown in Figure 2.

Moreover, the Luan system of Figure 2 that contains the Luan memory configuration controller is specifically designed to eliminate the additional memory of the prior art system because that additional memory is said to possibly "be quite large and is often times under-utilized if the peripheral associated with peripheral controller 106 does not require use of the entire memory space provided by memory 107. This under utilization of memory degrades system capability and increases the overall memory cost in a computer system." (Luan column 1 lines 38-43.) Thus, not only does Luan not teach use of an additional memory in the system of Figure 2, Luan actually teaches away from adding this type of additional memory to the system of Figure 2.

2. Applicants' control circuit receives a request for data, wherein a copy of the requested data may be stored within the first and the at least one additional storage device.

In contrast to Applicants' control circuit, when a memory configuration controller 202 of Luan Figure 2 receives a request for data via the shared memory bus 206 or the host processor bus 203, that request must be directed to the single memory 104 to which that memory configuration controller 202 is coupled. That is, there is no "additional storage device" coupled to the memory configuration controller 202 that may store the data.

3. Applicants' control circuit initiates at least one of a first reference to the first storage device and a second reference to the at least one additional storage device based on the state of the programmable indicator.

In contrast, a Luan memory configuration controller 202 does not initiate at least one of a first reference to the first storage device and a second reference to the at least one additional storage device as controlled by any programmable indicator. As previously stated, each memory configuration controller 202 is coupled to exactly one memory 104 that stores data. Thus, a given controller 202 only issues one memory reference to its respective memory 104. A controller 202 would never issue a "second reference to the at least one additional storage device", since a controller is not coupled to any additional memory. Moreover, any programmable indicator in Luan is provided to determine to which bus the memory configuration controller is coupled, and has nothing to do with how that memory configuration controller issues a request to its respective memory.

Finally, before continuing, it may be noted that the foregoing discussion is based on an understanding that the Examiner is citing a single instance of a Luan memory controller 202 as teaching Applicants' control circuit. According to a different interpretation of the rejection, the Examiner may be citing multiple Luan memory controllers 202 as collectively teaching Applicants' control circuit. Luan does not, according to this interpretation, teach Applicants' Claimed invention for at least the following reason. The various Luan memories 104 of Figure 2 each make up a portion of the entire main memory space. When a memory request is submitted to the Luan memory, the address submitted with that request, as well as the system configuration, will select one memory device 104 to which that request will be directed. (See, for example, Luan column 2 lines 3-7 and 13-24.) In other words, in Luan, copies of any requested data residing at a given address will not be stored within two different memories 104. Stated yet another way, data at some address X in the Luan memory space will be retrieved from exactly one of the memories 104, and will not be stored within two of the memories 104 such that a memory configuration controller 202 has a choice as to which of the memories may provide the data. Therefore, Luan does not teach a system wherein copies of any requested data may be retrieved from either a first or an additional storage device, as is claimed by Applicants' Claim 1.

To summarize, regardless of whether the Examiner cites one, or more than one, of the Luan memory configuration controllers 202 as teaching Applicants' control circuit, Luan does not teach Applicants' claimed invention of Claim 1, and Claim 1 is allowable over this rejection as presently presented.

Claims 3-4 and 6-10 depend from Claim 1 and are allowable for at least the reasons discussed above in regards to Claim 1. The Claims further include additional scopes and aspects not taught by Luan as follows:

Claim 3 describes the aspect wherein Applicants' control circuit will issue a second reference for the requested data to the additional memory only if the first reference to the first memory is not capable of being completed. The Examiner cites the following passage of Luan as teaching this aspect of Applicants' invention:

> "memory configuration controller 202 couples the memory I/O port to either the SMB 206 or to the HPB 203 respectively."

Thus, the Examiner appears to be citing the coupling of a given memory configuration controller 202 to one of the buses as teaching this aspect.

The cited passage has nothing to do with the memory configuration controller 202 issuing first and second references to two different memories, as is claimed in Applicants' Claims 1 and 3. Rather, it has to do with how the memory configuration controller is receiving a request (i.e., either via the SMB or the HPB.)

In addition to the foregoing, there is no need in Luan for any of the memory configuration controllers 202 to initiate both first and second references to two different memories 104 in attempt to retrieve copies of the requested data. This is because in Luan, there are not multiple copies of any requested data that are stored within two different memories, as is claimed by Applicants' Claim 1. As discussed above, each memory 104 in Luan provides a portion of the entire memory address space, and one memory is not storing any subset of data stored by a different memory 104.

Finally, in Luan, no determination is ever made that a first initiated reference to a first memory is not capable of fulfilling a request, as is claimed in

Claim 3. Each Luan reference (request) is routed to the appropriate memory configuration controller 202 based on the decoding of the address by address and command decoder 410, and further based on the system configuration determined when the system is started (see Luan column 2 lines 37-42.) Thus, Luan does not teach the aspect of Claim 3 related to making a determination as to whether a first initiated reference may be fulfilled.

For all of the additional reasons discussed above, Luan does not teach the additional aspects of Applicants' Claim 3, and Claim 3 is therefore allowable over this rejection.

Claim 4 describes the aspect wherein a second reference to the additional memory device is always issued regardless of whether that second reference is required to complete the request. The Examiner cites Table 2, which relates to how controller 303 (Figure 3) generates output enable and select signals for the memory 104 to which it is coupled. It is not understood how Table 2 in any way teaches that the Luan controller 202 initiates two different memory references to two different memory devices in order to retrieve requested data, as described by Applicants' Claim 4. In fact, Figure 3, which illustrates controller 303 of Table 2, clearly shows that the memory configuration controller 202 is coupled to exactly one memory 104, not at least two storage devices as claimed by Applicants' Claims 1 and 4. For at least this additional reason, it is submitted that Luan does not teach the additional aspects of Claim 4, and Claim 4 is allowable over this rejection for this additional reason.

Claim 7 describes the aspect wherein mode switch logic modifies the state of a programmable indicator if at least a first predetermined number of multiple requests require the second reference to complete. The Examiner states that this is taught by the discussion in Luan column 2 lines 33-45 of configuring the Luan system at system startup. At system start-up time, there is no information regarding how many requests that were issued to the memory required a second reference to complete. Thus, this passage could not possibly teach setting a mode based on such a number of requests. Moreover, the Luan system does not track how requests are completed, so there would not be any historical data

that could *ever* be used to trigger a mode switch operation, as is claimed by Applicants' Claim 7. Therefore, there can be no mode switch logic in Luan that changes the state of the indicators based on how many requests require a second reference to complete.

Finally, as previously discussed, the Luan system only initiates a single reference to retrieve data when a request is received. That reference will occur via either the SMB or the HPB as determined by the request address and system configuration. There is no reason in Luan to initiate two references to two different memories 104 to fulfill a given request, thus any aspect of Applicants' invention related to a "second reference" is not taught or even suggested by Luan.

Claim 8 describes modifying the state of an indicator if the multiple requests do not require the second reference to complete. For additional reasons that are similar to the reasons discussed above in regards to Claim 7, Claim 8 is allowable over this rejection.

Claim 9 describes the mode switch logic as including a circuit that allows the number of requests that result in a mode switch to be programmable. In Luan, there is no "mode switch logic" that switches modes based on the way requests were fulfilled in the past, as discussed above. In fact, this type of information is not even maintained in Luan. Therefore, Luan most certainly does not teach the aspect of allowing the predetermined numbers of past requests that control mode switching to be programmably selected.

Claim 10 depends from Claim 8 and is allowable for the additional reasons discussed in regards to Claim 8.

2. Claims 12-20 and 22-32 were rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 5,627,992 to Baror ("Baror"). This rejection is respectfully traversed.

Baror describes a cache system wherein the cache mode is programmable. When operating in a write-through mode, every write access is performed into the main memory. In the case of a cache hit, the data is also

written into the cache. (Baror column 6 lines 25-29.) In contrast, when operating in a copy-back mode, a write access is performed only in the cache for a cache hit. The block including the written data is marked as modified. The data is copied back to main memory when the modified block is replaced. (Baror column 4 lines 26-29.) The Examiner cites the aspect of configuring the cache according to write-though versus copy-back mode as teaching Applicants' control circuit of Claim 12. (Office Action page 5.)

The aspect cited by the Examiner relates to storing data to cache and/or memory. The control circuit of Claim 12, both as it was originally presented, and as it is now amended, describes a control circuit for retrieving requested data from one or both of two different memories based on a mode setting. (See Claim 12 line 11.) Thus, the cited aspect of Baror has nothing to do with Claim 12, both as currently and as previously presented.

Additionally, it may be noted that the Examiner cites the Baror memory address logic 305 of Figure 3 as teaching Applicant's first memory logic. (Office Action page 4 section 3.) Claim 12, both as previously presented and as currently presented, describes retrieving requested data from the first memory logic. (Claim 12 line 11.) The Baror memory address logic is described as follows:

> "The Memory Address Logic (MAL) includes two address incrementers. The first latches and increments the memory bus addresses for operation from the bus to the ICU. The second latches and increments the addresses for read operation initiated by the ICU. The MAL is shown in FIG. 3 as unit 305". (Baror column 15 lines 39-44.)

Thus, the MAL appears to be logic that generates the memory bus addresses, and does not appear to be any sort of logic that would store data, or from which requested data may be retrieved. If this rejection is maintained, more clarification is respectfully requested regarding the significance of the MAL as it relates to Applicants' first memory logic of Claim 12.

To summarize, none of the passages of Baror cited by the Examiner, nor anything else in Baror, teaches the aspects of Claim 12. Therefore, this rejection

is improper, and should be withdrawn. Claim 12 is allowable as presently presented.

Claims 13-20 depend from Claim 12 and are allowable for at least the reasons discussed above in regards to Claim 12. These Claims include additional aspects of Applicants' invention not taught by Baror, as follows:

Claim 14 further describes a circuit that determines whether a programmable indicator is in a first state, and whether the other memory must be referenced to complete the request, and if not, to obtain the requested data from the first memory logic. The Examiner cites the Baror control circuit for placing the ICU in either copy-back or write-through mode, and wherein the control circuit is further configured to be responsive to the TLB write policy field. (Office Action page 5.) Again, this Baror operation of performing a write-through or copy-back operation has nothing whatsoever to do with data retrieval from two different storage devices. Moreover, the cited passage does not relate in any way to determining whether any particular storage device must be referenced to complete the data retrieval request. For this additional reason, Claim 14 is allowable over this rejection.

Claim 15 further describes a control circuit that initiates references to both the first memory logic and the at least one other memory if the at least one other memory must be referenced to complete the data retrieval request.

As noted above in regards to Claim 12, the Examiner cites memory address logic (MAL) 305 as teaching Applicants' first memory logic. Baror does not teach initiating a reference to this MAL, which is logic to generate addresses. This logic does not store data, and therefore a data retrieval operation would not be initiated to the MAL. Moreover, Baror does not teach any circuit for determining whether the at least one other memory must be referenced to complete the data retrieval request, and for then initiating data retrieval references based on an identified mode and on that determination. For these additional reasons, Claim 15 is allowable over that rejection.

Claim 16 relates to a control circuit that determines whether the indicator is in a predetermined state, and if so, the control circuit initiates a reference to

the first memory logic and the at least one other memory regardless of whether a reference to the other memory is needed. The Examiner states that this is taught by a passage in Baror that states:

> "wherein said cache control unit is configured to set said state of said cache block statue field to indicate said write-through write mode if said one or more write policy pins are placed in said first write policy pin state, even if said TLB write policy field is set in said second TLB write policy state."

(Office Action page 6 referencing column 52 lines 59-64 of Baror.) It is not understood how this passage relates in any way to Claim 16, which describes referencing both the first memory logic and the at least one other memory to retrieve data, regardless of whether the second reference is required to complete this data retrieval operation. The aspects of Claim 16 are not taught by Baror, and for this additional reason, Claim 16 is allowable over this rejection.

Claim 17 describes that if an indicator is in a predetermined state indicating the first memory logic is unavailable for storing data, the reference to the at least one other memory is initiated. Continuing the Examiner's analysis from Claim 12, the Examiner states that the MAL 305 of Baror Figure 3 teaches Applicants' first memory logic. (Office Action page 5.) However, the MAL does not store data. Moreover, nothing in Baror ever contemplates the scenario wherein the MAL would be unavailable. In fact, it appears the MAL must be available for the system to be operational. Thus, according to the Examiner's analysis from Claim 12, Baror does not teach this aspect of Applicants' invention.

The foregoing analysis of Claim 17 follows the Examiner's reasoning set forth in regards to Claim 12, from which Claim 17 depends. It does not appear that the Examiner continues his own line of reasoning, however. In particular, the Examiner now cites column 13 lines 7-13 as teaching the aspects of Claim 17. That passage refers to a synchronous ICU output pin that indicates the program mode of the processor, which may be either supervisor or user mode. This output is provided during a memory access during appropriate transactions. This appears to have nothing whatsoever to do with the MAL 305, which the

Examiner previously cited as teaching Applicants' first memory logic. Furthermore, it is not understood how this relates to initiating a data retrieval operation to a memory if some other memory is not available.

To summarize, the rejection of Claim 17 is not understood, and more clarification as to the significance of the cited passages of Baror is respectfully requested if this rejection is maintained.

Claim 18 describes that the first memory logic includes a shared cache, and wherein the at least one other memory includes one or more dedicated caches coupled to at least one instruction processor.

Recall that in regards to Claim 12, the Examiner cites the MAL 305 as teaching Applicants' first memory logic. The MAL most certainly does not include a shared cache. However, the Examiner does not appear to continue this analysis in regards to Claim 18. Instead, the Examiner cites column 7 lines 11-20 as teaching this aspect. This passage discusses the "Shared" status assigned to a cached block to indicate that more than one processor is using the data in that block. Another "Shared modified" status is assigned when data stored within the cache block has been modified. This has nothing whatsoever to do with teaching that the first memory logic is a shared cache, and the at least one other memory includes one or more dedicated caches. Nothing in Baror, including the cited passage, teaches the aspect of Claim 18, and for this additional reason, Claim 18 is allowable over this rejection.

Claim 19 describes that the main memory is coupled to the first memory logic to issue the request for data. The Examiner cites column 45 lines 40-42, which states that there is logic that should be capable of monitoring all main memory accesses. This cited Baror passage has nothing to do with the main memory issuing a request to some other memory (e.g., a cache) to retrieve data for that other memory. For this additional reason, Claim 19 is allowable over this rejection.

Turning next to independent Claim 22, this Claim, both as originally and currently presented, describes aspects similar to those discussed above in regards to Claim 12. In particular, this Claim describes attempting to retrieve

requested data from a first memory, at least one other memory, or from both memories based on a reference mode. The Examiner again cites the Baror discussion on write-through mode, which relates to a method of storing data to cache. This cited passage, as well as the remainder of the Baror reference, do not teach or suggest Applicants' invention of Claim 22.

Claims 23-29 depend from Claim 22 and are allowable for at least the reasons discussed above in regards to Claims 12 and 22. These Claims include additional aspects of Applicants' invention similar to those discussed above in regards to Claims 13-20, and are allowable for the additional reasons similar to those discussed above.

Independent Claim 30 describes aspects similar to those discussed above in regards to Claims 12 and 22. For example, as originally and currently presented, this Claim includes programmable storage means for storing control signals to control the way in which data is retrieved from first and second cache means (Claim 30 lines 6-7.) This Claim further describes initiating reference(s) to retrieve data from one or both of first and second cache means. This is not taught by Baror.

In addition to the foregoing, Claim 30 describes first and second cache means that receives **requests *from* the main memory** to initiate ***retrieval*** of the data. The Examiner asserts that this aspect is taught by a control circuit of Baror that performs a write-through operation. (Office Action page 9.) As stated above, that write-through operation involves storing, not retrieving data. Moreover, that write-through operation is initiated by a request from a processor, and not a request from a main memory, as follows:

> "When a write-through policy is selected, **every *processor write* to** the ICU is also written to the memory." (Baror column 19 lines 57-58, emphasis added.)

Therefore, Baror does not teach a system wherein first and second cache means receives data retrieval requests from a main memory, and for this additional reason, Claim 30 is allowable over this rejection, which should be withdrawn.

Claims 31-32 depend from Claim 30 and are allowable for at least the reasons discussed above in regards to Claim 30. These Claims include additional aspects of Applicants' invention not taught by Baror, as follows:

Claim 31 describes mode switching means for monitoring system conditions and automatically altering one or more of the control signals based on the system conditions. This alters the mode that determines whether the first and/or second cache means are referenced to retrieve requested data.

The Examiner cites using the Baror preload instruction as part of a context switch procedure as teaching this aspect of the invention. As known in the art, context switching refers to a process of storing and restoring the state of a CPU so that multiple processes (e.g., threads) can share a single CPU resource in a multitasking environment. The Baror preload instruction can facilitate context switching by loading the cache with specific data variables or instructions before they are needed. It is not understood how this type of discussion in Baror in any way teaches Applicants' Claim 31, which relates to automatically switching a mode that controls referencing of first and/or second cache means. Nothing in Baror teaches the claimed aspect of the invention, and for this additional reason, Claim 31 is allowable over this rejection.

3. Claims 2 and 5 were rejected under 35 USC §103(a) as being unpatentable by Luan. This rejection is respectfully traversed.

Claim 2 depends from Claim 1 and is allowable over this rejection for all of the reasons set forth above in regards to this Claim.

Claim 2 further describes the aspect wherein the control circuit initiates the first and second references in a time-order controlled by the state of the programmable indicator. That is, the first reference may be initiated first or vice versa.

In regards to this aspect of the invention, the Examiner asserts that "stating that there is a sequence in which things must occur does not change the purpose or functionality of the claimed invention. Therefore, it would have been obvious to one of ordinary skill in the art to enable Luan's 'shared Memory' to

have the indicator controlled by a time order and by changing state orders". (Office Action page 2, last couple of sentences.)

In regards to the Examiner's first assertion, the sequence in which things are ordered (i.e., whether Applicants' first or second reference occurs first) affects how quickly the data can be returned to the requester. Indeed, this control over the sequence of references is a significant benefit provided by Applicants' invention. For example, Applicants' Specification describes that operation efficiency may be improved by selecting shared-cache mode (wherein the shared cache logic is referenced first) if the shared caches are relatively large as compared to the dedicated cache memories of the processors. In contrast, as the relative size of the dedicated caches increase as compared to the shared cache, it becomes more likely that efficiency will be improved by switching to a processor-bus mode wherein the processor caches are referenced first. (Specification page 6 lines 6-10.) Thus, this aspect most certainly changes the purpose or functionality of the claimed invention. Without this functionality, the system will likely not run at maximum efficiency, as is the case with prior art systems.

In regards to the Examiner's second assertion, the Luan system does not issue first and second references to two different memories to retrieve the same data, since data is not stored in duplicate within the Luan memory. In other words, in Luan, a request issued by either a CPU or a peripheral device to retrieve data from the Luan memory does not result in multiple references to multiple memories 104. Thus, there would be absolutely no motivation to provide an indicator to control a time-order between first and second references. For these additional reasons, Claim 2 is allowable over this rejection, which is improper, and should be withdrawn.

Finally, the Examiner cites several references that are said to stand for the proposition that an order of performing processing steps when making certain manufactured articles (e.g., a laminated sheet material) is prima facie obvious in the absence of new or unexpected results. It is hard to understand how these cases relate in any way to Applicants' system of Claim 2 that allows for

programmably selecting an order in which two different storage devices are referenced after a data retrieval request is received.

Turning next to Claim 5, this Claim describes the second reference as being issued before the first reference if the programmable indicator is in the second state. The Examiner rejects this Claim for reasons similar to those set forth in regards to the rejection of Claim 2. For all of the reasons discussed in regards to Claim 2, Luan does not even begin to suggest Applicants' invention of Claim 5, particular since there is never a "second reference" to a second memory in Luan when a request for data is received.

4. Claim 11 was rejected under 35 USC §103(a) as being unpatentable over Luan in view of Baror. This rejection is respectfully traversed.

Claim 11 depends from Claim 1 and is allowable for at least the reasons set forth in regards to Claim 1. In addition, Claim 11describes the aspect wherein a request that is issued from main memory is requesting retrieval of data associated with one or more incomplete memory coherency actions. A tracking circuit is utilized to track these incomplete memory coherency actions such that data is returned to the main memory only after all of these actions are completed.

In regards to this aspect of the invention, the Examiner states that although Luan fails to teach the aspects of Claim 11, the Baror disclosure teaches the use of ownership. The Examiner further asserts that there are several ownership schemes, and it would have been obvious to one of ordinary skill in the art in view of the general ownership discussion in Baror to utilize Applicants' tracking device.

Applicants' representative disagrees with the Examiner's assessments. First of all, nothing in Baror appears to discuss a cache receiving a request from main memory for the return of data. Secondly, many ways of maintaining coherency have been devised, and the mere mention of ownership in Baror does not rending obvious Applicants' request tracking circuit that is used when data is being returned from a storage device such as a cache back to a main memory. For this additional reason, Claim 11 is allowable over this rejection.

5. Claim 21 was rejected under 35 USC §103(a) as being unpatentable over Baror. This rejection is respectfully traversed. Claim 21 describes a mode switch logic that monitors conditions within the memory system and automatically re-programs the indicator based on these conditions.

The Examiner states that the claimed aspects of Claim 21 are taught by Baror column 17 lines 21-25, which relates to the chip select mapping register. This register has nothing to do with switching the mode that controls how two different storage devices (i.e., the first memory logic and/or the at least one other memory) are accessed. Additionally, Baror does not even begin to suggest that this register "monitors conditions with the memory system". Nor does Baror suggest that this register is loaded automatically.

In this regard, the Examiner states that having something done automatically does not change the purpose or functionality of the claimed invention. This statement is not understood. Many inventions have as their sole purpose the function of performing something automatically that previously was only done manually. Therefore, this type of an aspect most certainly relates to an aspect of the invention that is patentable over and above that described in the corresponding independent Claim. Moreover, Applicants' are claiming both the automated aspect of the mode switching, as well as the function of monitoring conditions within the memory system so that the mode switching can be based on those monitored conditions. None of these aspects is even suggested by Baror. Therefore, Claim 21 is allowable over this rejection.

Conclusion

In the Office Action dated 11/28/2005, Claims 1-32 were rejected. In the Amendment set forth above, Claim 1, 12, 22, and 30 is amended, and the remaining Claims are as originally presented. In view of the amendments to the Claims and the remarks set forth herein, it is respectfully submitted that all Claims are in condition for Allowance, and a Notice of Allowance is respectfully requested. If the Examiner has any questions regarding the subject Application or this response, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,

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